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JUL 24 2006
PATENT & TRADEMARK OFFICE

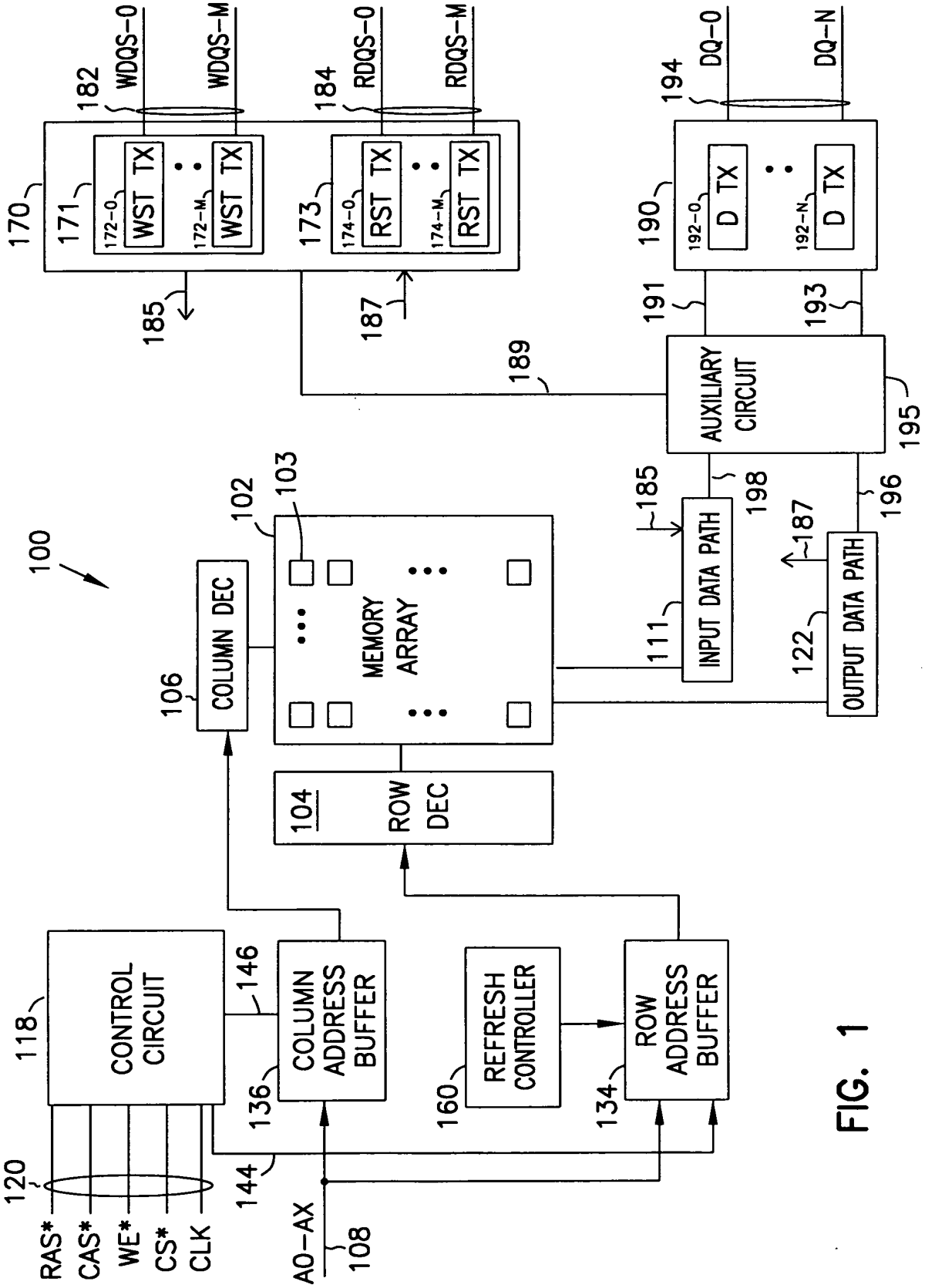


FIG. 1

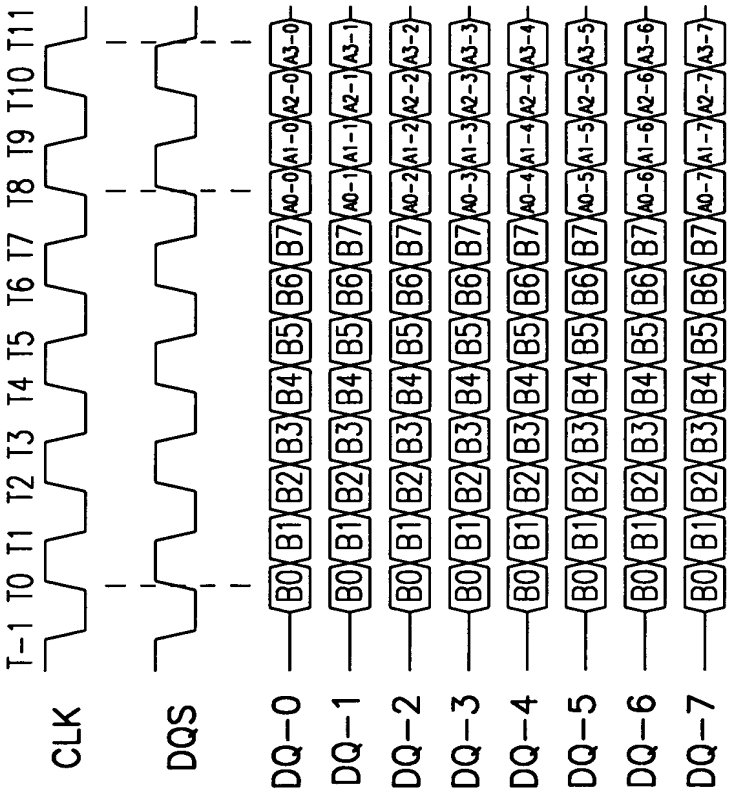

T-1 T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11
CLK
DQS
DQ-0
DQ-1
DQ-2
DQ-3
DQ-4
DQ-5
DQ-6
DQ-7
B0 B1 B2 B3 B4 B5 B6 B7
A0-0 A1-0 A2-0 A3-0
A0-1 A1-1 A2-1 A3-1
A0-2 A1-2 A2-2 A3-2
A0-3 A1-3 A2-3 A3-3
A0-4 A1-4 A2-4 A3-4
A0-5 A1-5 A2-5 A3-5
A0-6 A1-6 A2-6 A3-6
A0-7 A1-7 A2-7 A3-7

FIG. 2

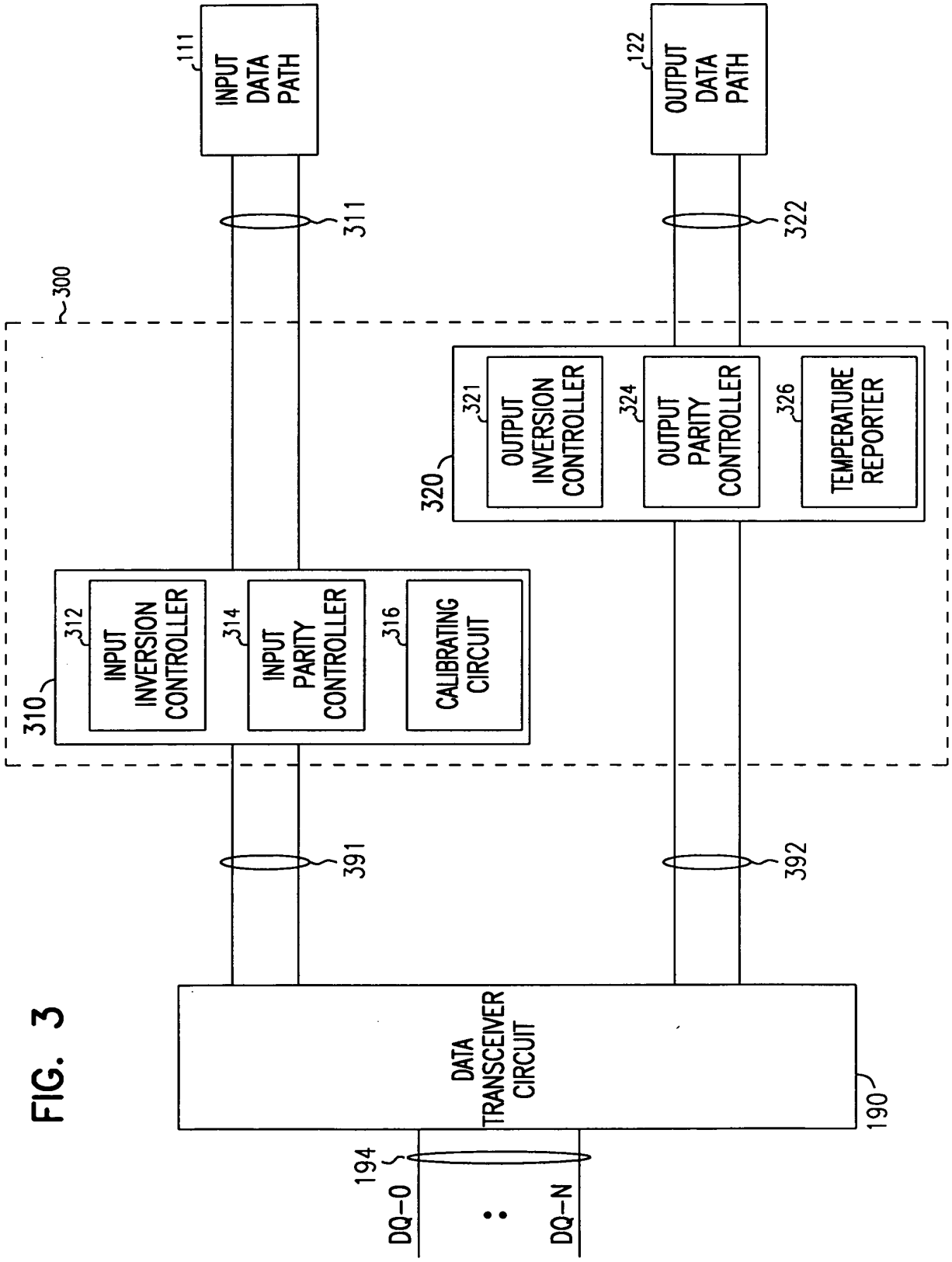

111
INPUT DATA PATH
122
OUTPUT DATA PATH
311
322
300
321
OUTPUT INVERSION CONTROLLER
324
OUTPUT PARITY CONTROLLER
326
TEMPERATURE REPORTER
320
312
INPUT INVERSION CONTROLLER
314
INPUT PARITY CONTROLLER
316
CALIBRATING CIRCUIT
310
391
392
DATA TRANSCEIVER CIRCUIT
190
194
DQ-0
DQ-N

FIG. 3

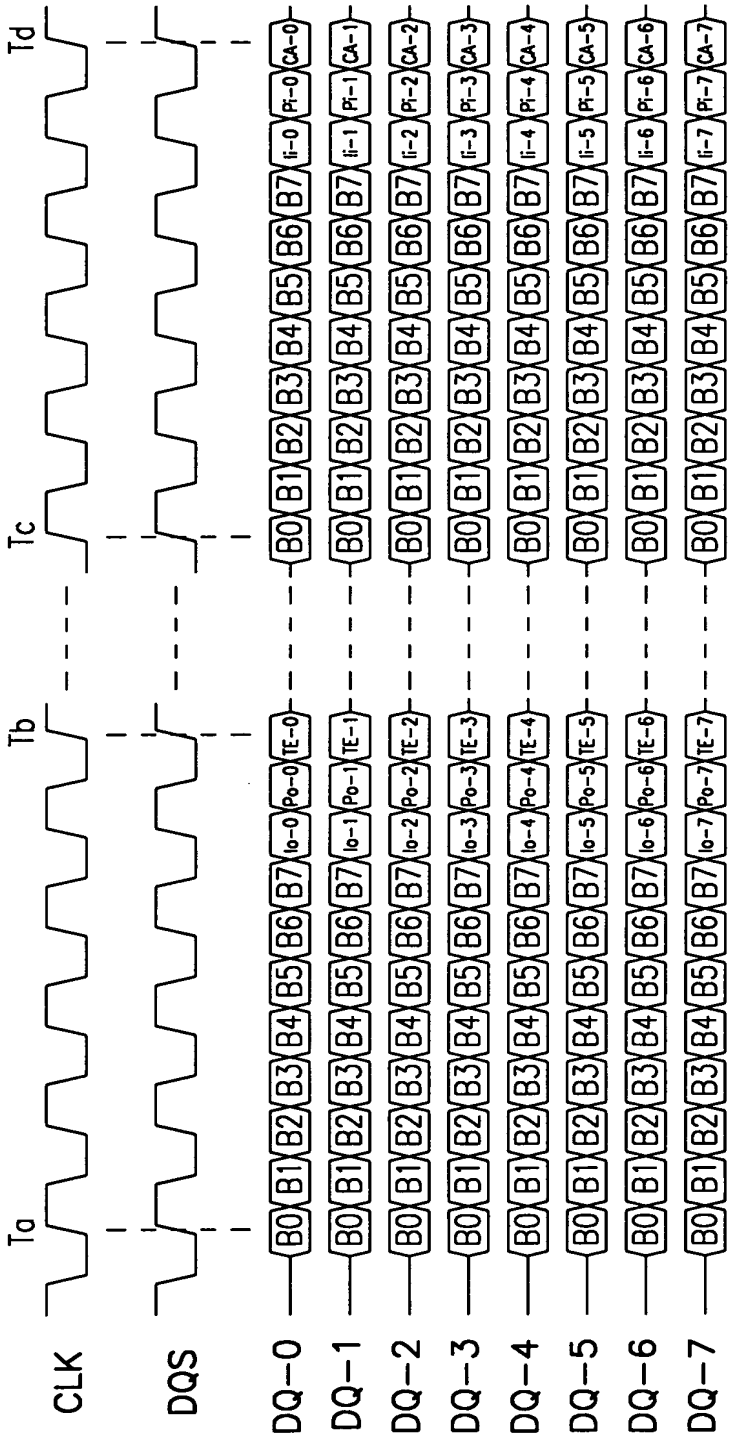

Ta
Tb
Tc
Td
CLK
DQS
DQ-0
DQ-1
DQ-2
DQ-3
DQ-4
DQ-5
DQ-6
DQ-7
B0 B1 B2 B3 B4 B5 B6 B7
Io-0 Po-0 TE-0
Ii-0 Pi-0 CA-0
Io-1 Po-1 TE-1
Ii-1 Pi-1 CA-1
Io-2 Po-2 TE-2
Ii-2 Pi-2 CA-2
Io-3 Po-3 TE-3
Ii-3 Pi-3 CA-3
Io-4 Po-4 TE-4
Ii-4 Pi-4 CA-4
Io-5 Po-5 TE-5
Ii-5 Pi-5 CA-5
Io-6 Po-6 TE-6
Ii-6 Pi-6 CA-6
Io-7 Po-7 TE-7
Ii-7 Pi-7 CA-7

FIG. 4

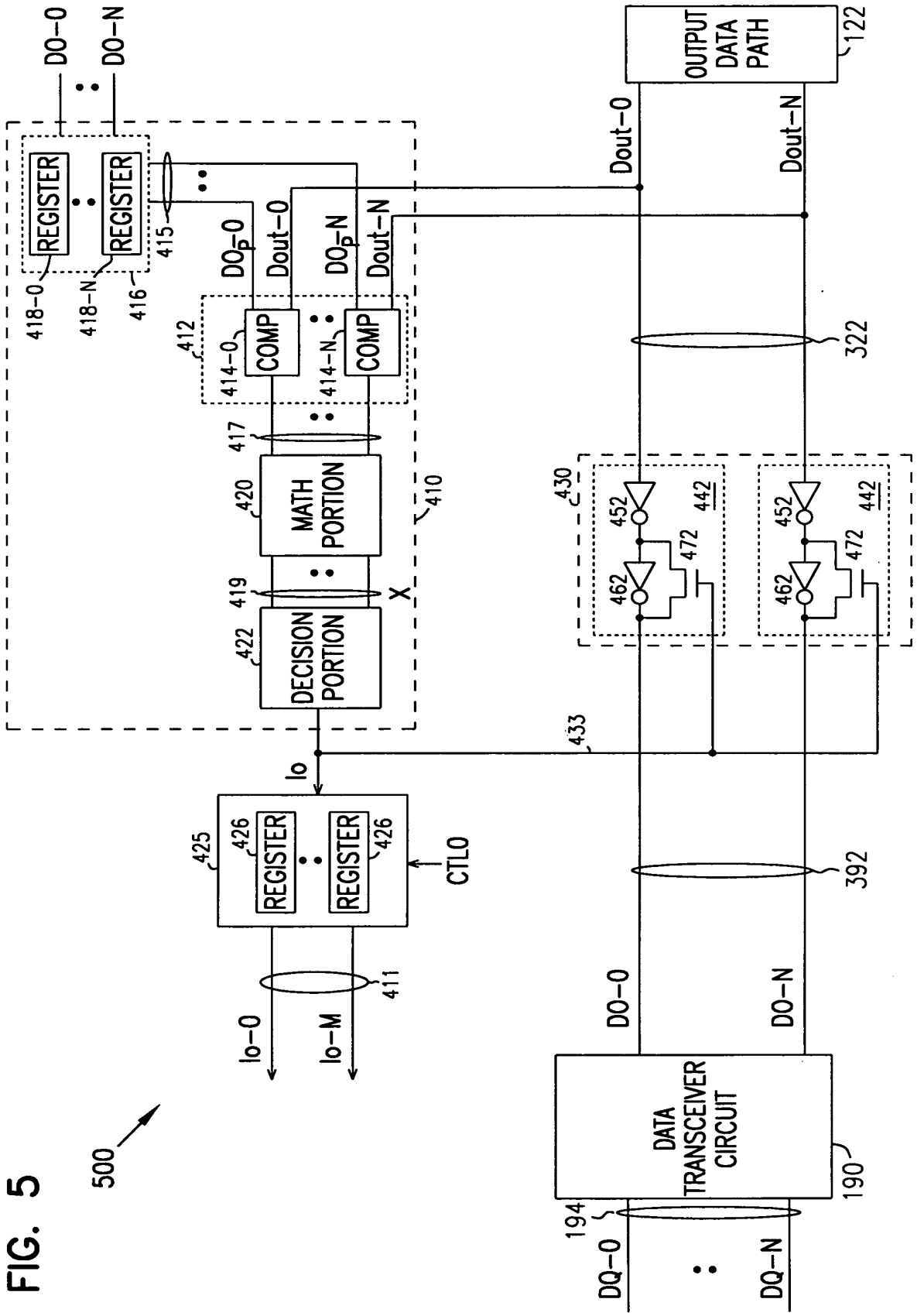

DO-0
DO-N
REGISTER
REGISTER
415
418-0
418-N
416
412
414-0
414-N
COMP
COMP
DOp-0
Dout-0
DOp-N
Dout-N
417
420
MATH PORTION
419
422
DECISION PORTION
410
X
Io
425
426
REGISTER
REGISTER
CTLO
411
Io-0
Io-M
500
OUTPUT DATA PATH
122
Dout-0
Dout-N
322
430
452
442
462
472
433
392
DO-0
DO-N
DATA TRANSCEIVER CIRCUIT
190
194
DQ-0
DQ-N

FIG. 5

		B0 B0 B0 B0 B0 B0 B0 B0			
	DO_P	00000111	Io	X	Y
ROW 1	Dout−0 TO Dout−7	11111000	1	8	
	INVERTED (Dout−0 TO Dout−7)	00000111			0
		11110000	1	7	
		00001111			1
		11100000	1	6	
		00011111			2
		11000000	1	5	
		00111111			3
		10000000	0	4	
		01111111			4
ROW 6	Dout−0 TO Dout−7	00000000	0	3	
	INVERTED (Dout−0 TO Dout−7)	11111111			5
		00000001	0	2	
		11111110			6
		00000011	0	1	
		11111100			7
		00000111	0	0	
		11111000			8
		00001111	0	1	
		11110000			7
		00011111	0	2	
		11100000			6
		00111111	0	3	
		11000000			5
		01111111	0	4	
		10000000			4
		11111111	1	5	
		00000000			3
		11111110	1	6	
		00000001			2
ROW 16	Dout−0 TO Dout−7	11111100	1	7	
	INVERTED (Dout−0 TO Dout−7)	00000011			1

FIG. 6

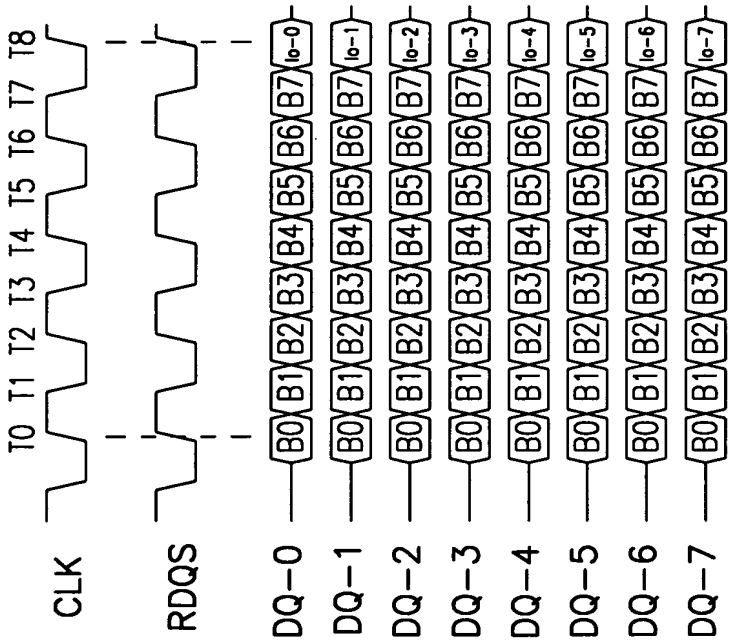

T0 T1 T2 T3 T4 T5 T6 T7 T8
CLK
RDQS
DQ-0
DQ-1
DQ-2
DQ-3
DQ-4
DQ-5
DQ-6
DQ-7
B0 B1 B2 B3 B4 B5 B6 B7 Io-0
B0 B1 B2 B3 B4 B5 B6 B7 Io-1
B0 B1 B2 B3 B4 B5 B6 B7 Io-2
B0 B1 B2 B3 B4 B5 B6 B7 Io-3
B0 B1 B2 B3 B4 B5 B6 B7 Io-4
B0 B1 B2 B3 B4 B5 B6 B7 Io-5
B0 B1 B2 B3 B4 B5 B6 B7 Io-6
B0 B1 B2 B3 B4 B5 B6 B7 Io-7

FIG. 7

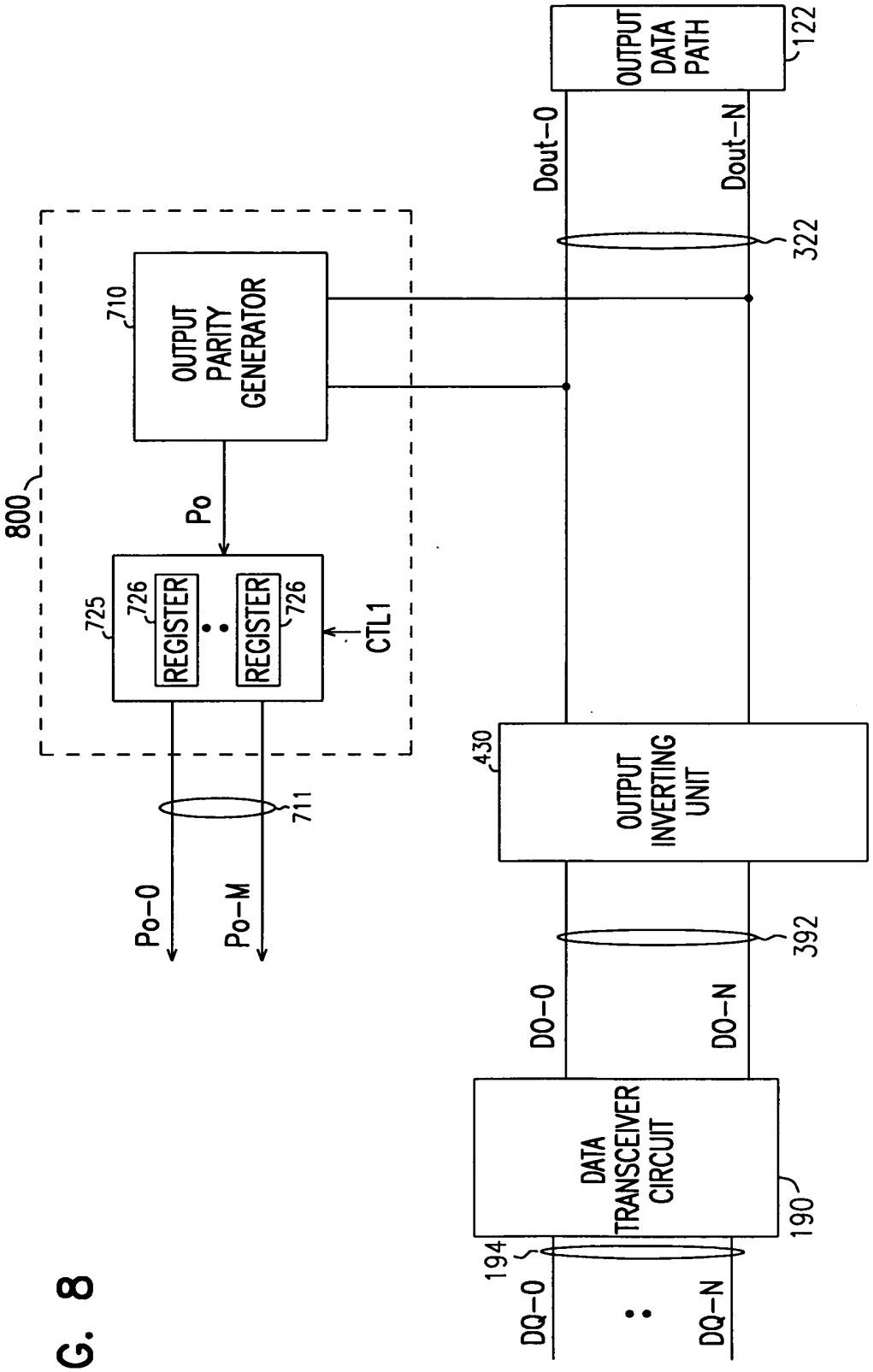

OUTPUT DATA PATH
122
Dout-0
Dout-N
322
OUTPUT PARITY GENERATOR
710
800
Po
725
726
REGISTER
REGISTER
726
CTL1
711
Po-0
Po-M
OUTPUT INVERTING UNIT
430
392
DO-0
DO-N
DATA TRANSCEIVER CIRCUIT
190
194
DQ-0
DQ-N

FIG. 8

	Dout-0 TO Dout-7 B0 B0 B0 B0 B0 B0 B0 B0	PO
ROW 1	00000000	0
	00000001	1
ROW 3	00000011	0
	00000111	1
	00001111	0
ROW 6	00011111	1
	00111111	0
	01111111	1
	11111111	0
	11111110	1
	11111100	0
	11111000	1
	11110000	0
ROW 14	11100000	1
	11000000	0
	10000000	1

FIG. 9

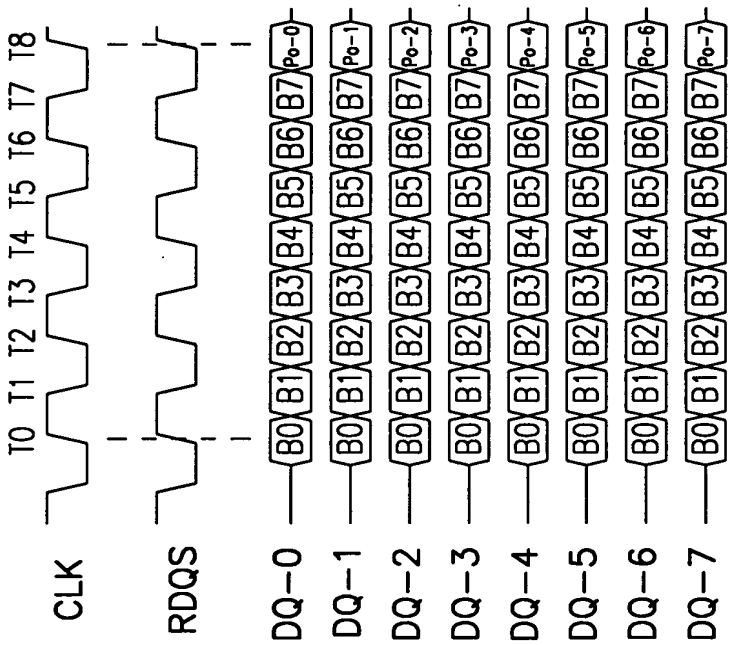

T0 T1 T2 T3 T4 T5 T6 T7 T8
CLK
RDQS
DQ-0
DQ-1
DQ-2
DQ-3
DQ-4
DQ-5
DQ-6
DQ-7
B0 B1 B2 B3 B4 B5 B6 B7
Po-0
Po-1
Po-2
Po-3
Po-4
Po-5
Po-6
Po-7

FIG. 10

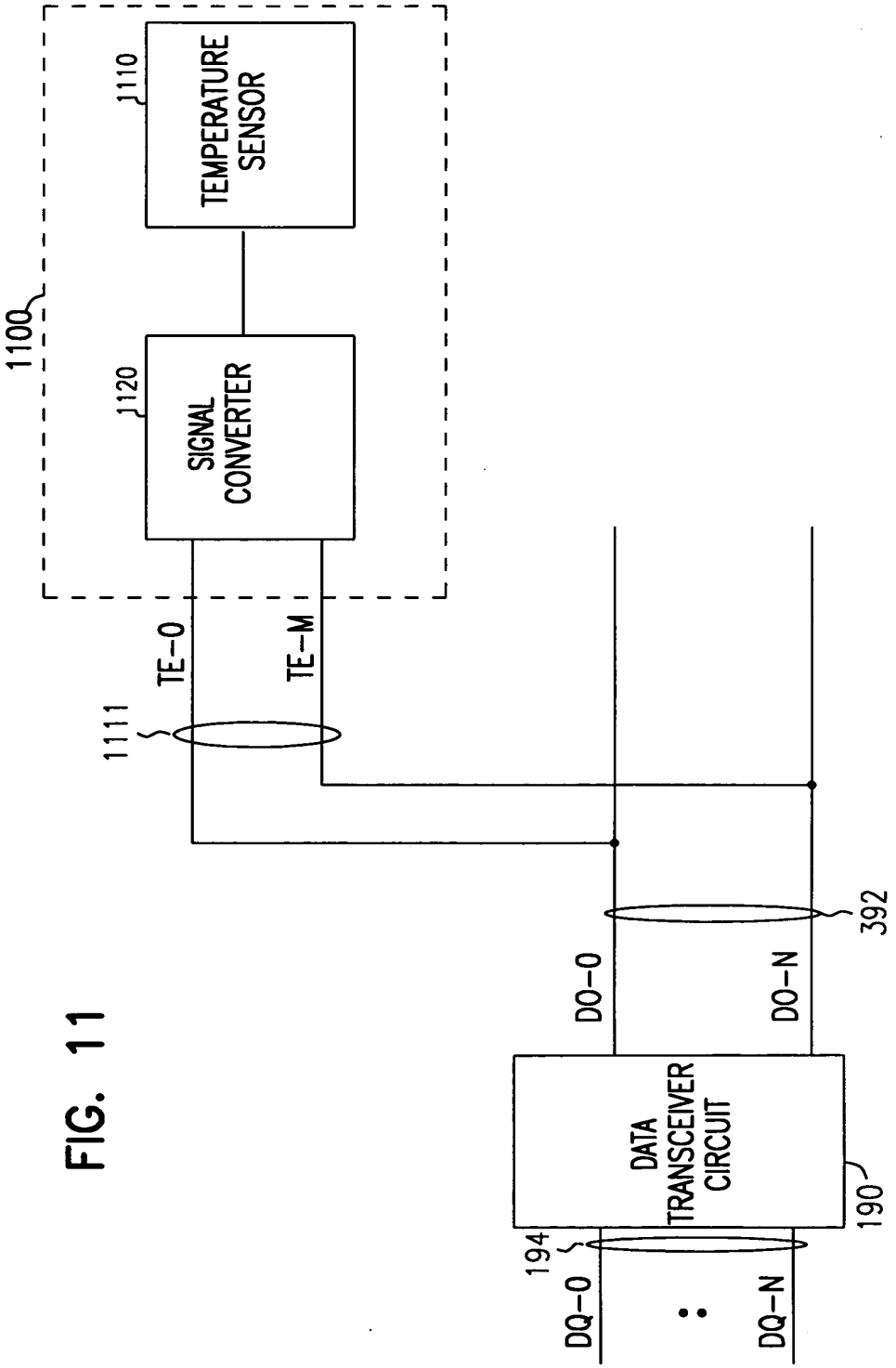

1100
1110
TEMPERATURE SENSOR
1120
SIGNAL CONVERTER
TE-0
TE-M
1111
392
DO-0
DO-N
DATA TRANSCEIVER CIRCUIT
190
194
DQ-0
DQ-N

FIG. 11

BITS	TMP	TMP	TMP	TMP	TMP	TMP	TMP	TMP
TE-0	0	0	0	0	0	0	0	0
TE-1	0	0	0	0	0	0	1	1
TE-2	0	0	0	0	0	1	1	1
TE-3	0	0	0	0	1	1	1	1
TE-4	0	0	0	1	1	1	1	1
TE-5	0	0	0	1	1	1	1	1
TE-6	0	0	1	1	1	1	1	1
TE-7	0	1	1	1	1	1	1	1
TEMP °C	0	15	30	45	60	75	90	105

COL1 COL2 COL3 COL4 COL5 COL6 COL7 COL8

FIG. 12

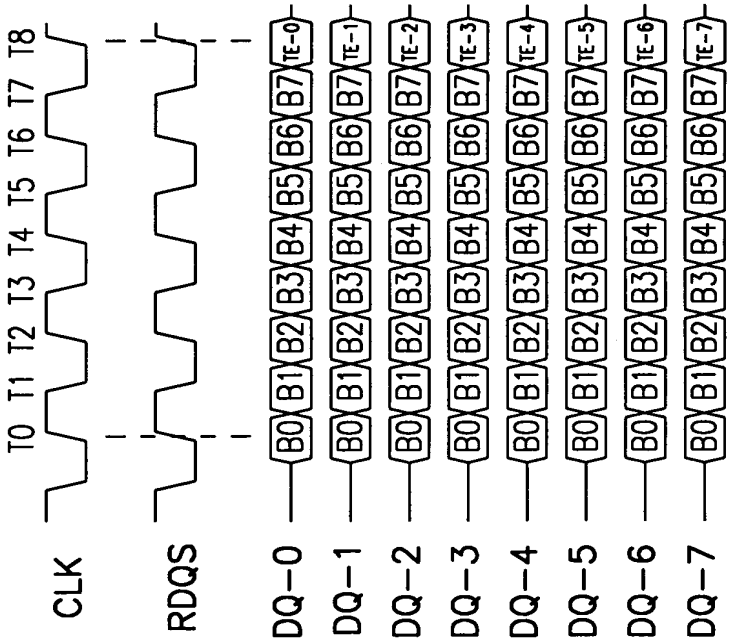

T0 T1 T2 T3 T4 T5 T6 T7 T8
CLK
RDQS
DQ-0
DQ-1
DQ-2
DQ-3
DQ-4
DQ-5
DQ-6
DQ-7
B0 B1 B2 B3 B4 B5 B6 B7 TE-0
B0 B1 B2 B3 B4 B5 B6 B7 TE-1
B0 B1 B2 B3 B4 B5 B6 B7 TE-2
B0 B1 B2 B3 B4 B5 B6 B7 TE-3
B0 B1 B2 B3 B4 B5 B6 B7 TE-4
B0 B1 B2 B3 B4 B5 B6 B7 TE-5
B0 B1 B2 B3 B4 B5 B6 B7 TE-6
B0 B1 B2 B3 B4 B5 B6 B7 TE-7

FIG. 13

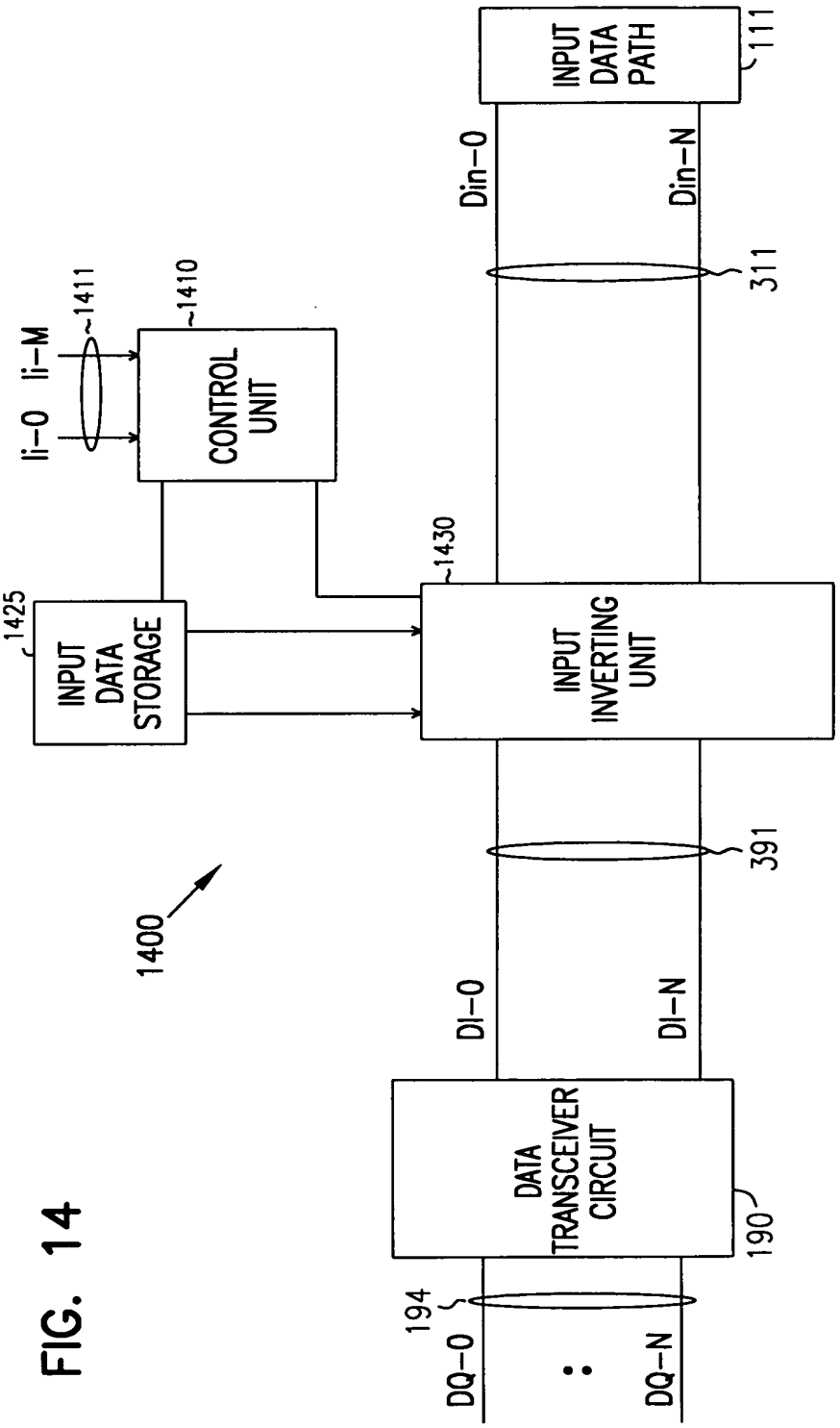

INPUT DATA PATH
111
Din-0
Din-N
311
1411
1410
Ii-0 Ii-M
CONTROL UNIT
1430
1425
INPUT DATA STORAGE
INPUT INVERTING UNIT
391
1400
DI-0
DI-N
DATA TRANSCEIVER CIRCUIT
190
194
DQ-0
DQ-N

FIG. 14

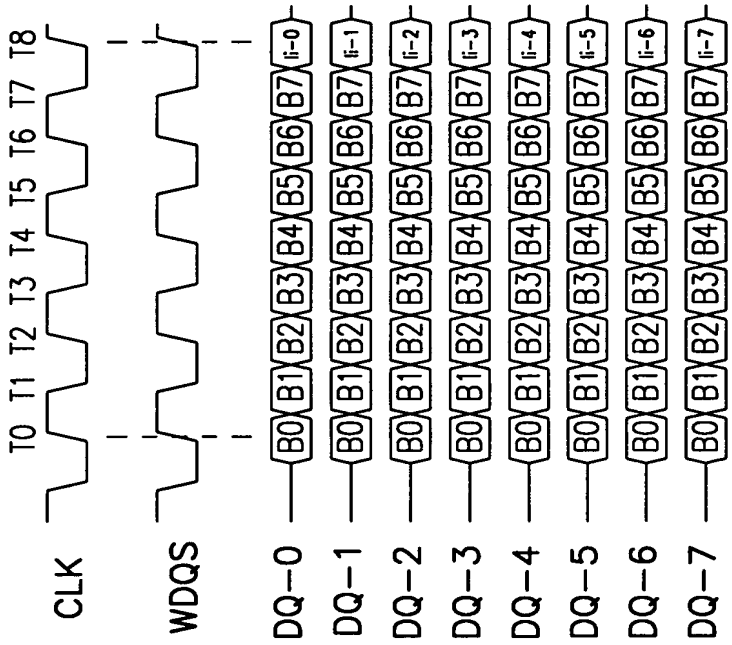

T0 T1 T2 T3 T4 T5 T6 T7 T8
CLK
WDQS
DQ-0
DQ-1
DQ-2
DQ-3
DQ-4
DQ-5
DQ-6
DQ-7
B0 B1 B2 B3 B4 B5 B6 B7
i=0
i=1
i=2
i=3
i=4
i=5
i=6
i=7

FIG. 15

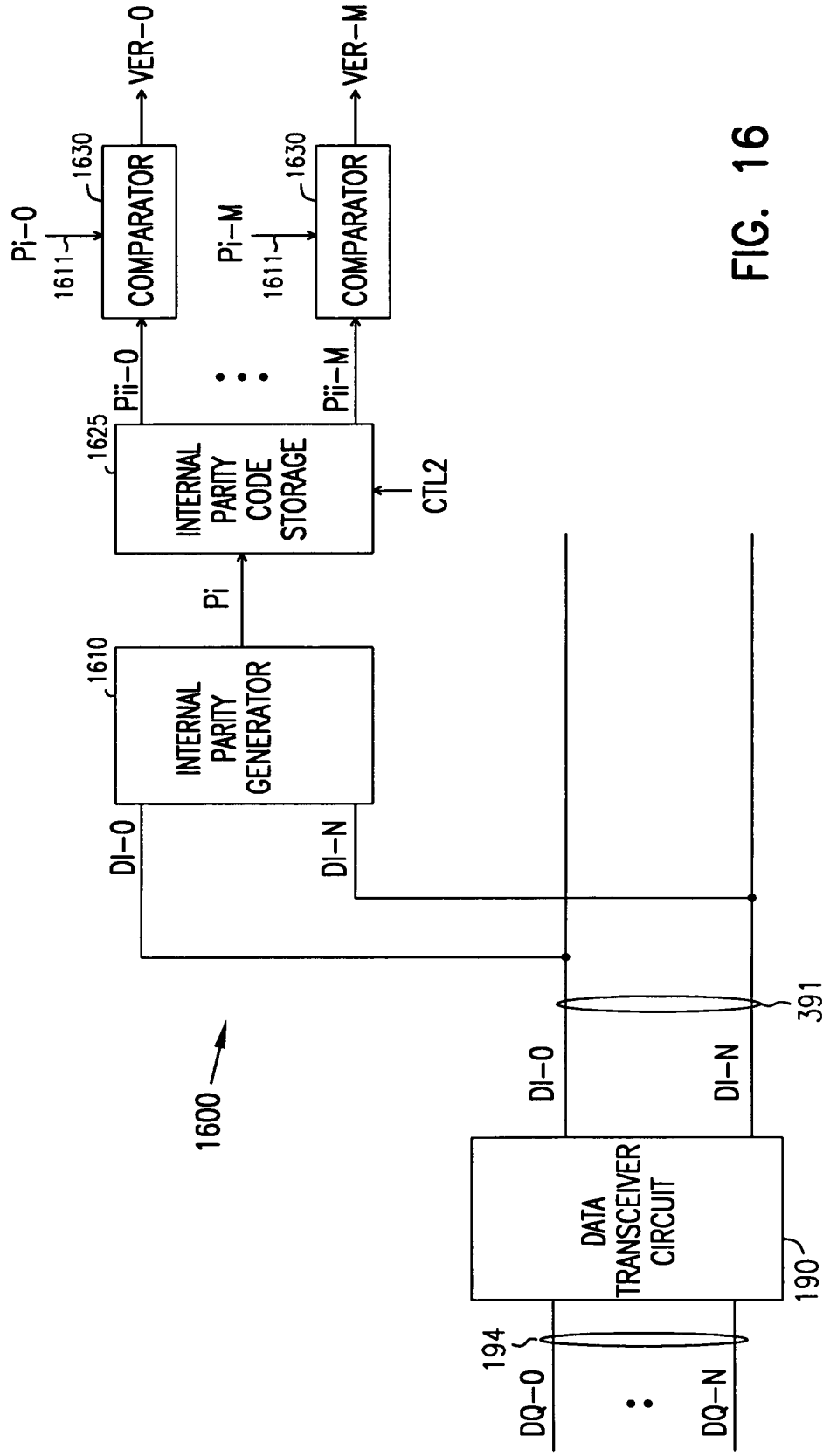

1600
1610
INTERNAL PARITY GENERATOR
Pi
1625
INTERNAL PARITY CODE STORAGE
CTL2
Pii-0
Pii-M
1630
COMPARATOR
1611
Pi-0
Pi-M
VER-0
VER-M
DI-0
DI-N
391
DATA TRANSCEIVER CIRCUIT
190
194
DQ-0
DQ-N

FIG. 16

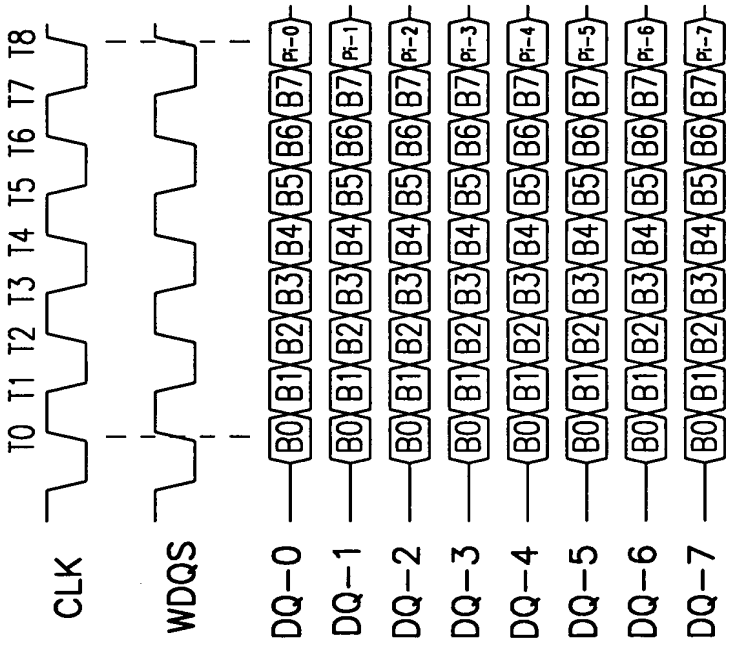
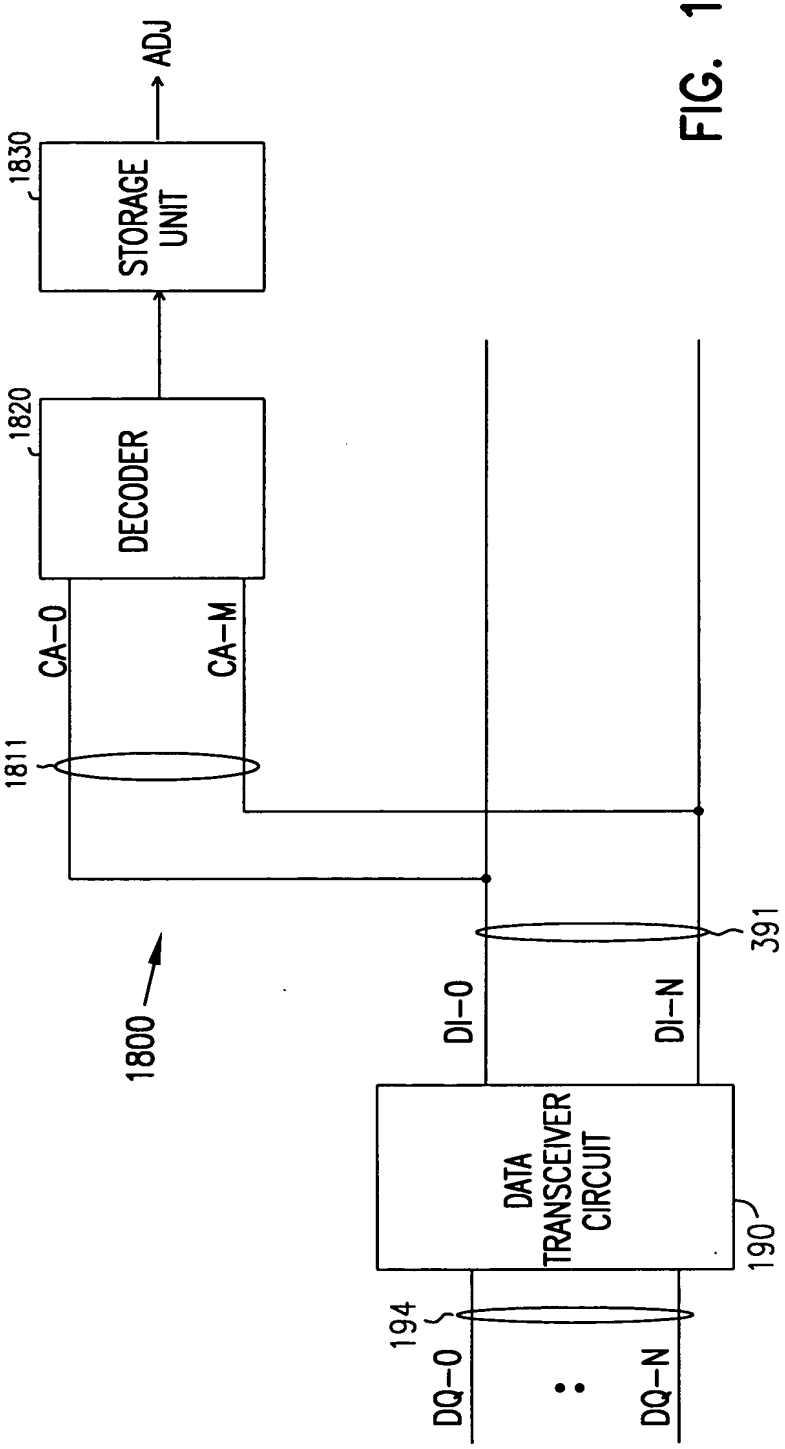

T0 T1 T2 T3 T4 T5 T6 T7 T8
CLK
WDQS
DQ-0
DQ-1
DQ-2
DQ-3
DQ-4
DQ-5
DQ-6
DQ-7
B0 B1 B2 B3 B4 B5 B6 B7
Fi-0
Fi-1
Fi-2
Fi-3
Fi-4
Fi-5
Fi-6
Fi-7

FIG. 17

FIG. 18


ADJ
1830
STORAGE UNIT
1820
DECODER
CA-0
CA-M
1811
1800
391
DI-0
DI-N
DATA TRANSCEIVER CIRCUIT
190
194
DQ-0
DQ-N

BITS	CAL	COL1	COL2	COL3	COL4	COL5	COL6	COL7	COL8	CAL
CA-0	0	0	0	0	0	0	0	0	0	0
CA-1	0	0	0	0	0	0	0	0	1	1
CA-2	0	0	0	0	0	0	0	1	1	1
CA-3	0	0	0	0	0	0	1	1	1	1
CA-4	0	0	0	0	0	1	1	1	1	1
CA-5	0	0	0	0	1	1	1	1	1	1
CA-6	0	0	0	1	1	1	1	1	1	1
CA-7	0	1	1	1	1	1	1	1	1	1
DELAY	-200	-150	-150	-100	-50	50	100	150	200	200

FIG. 19

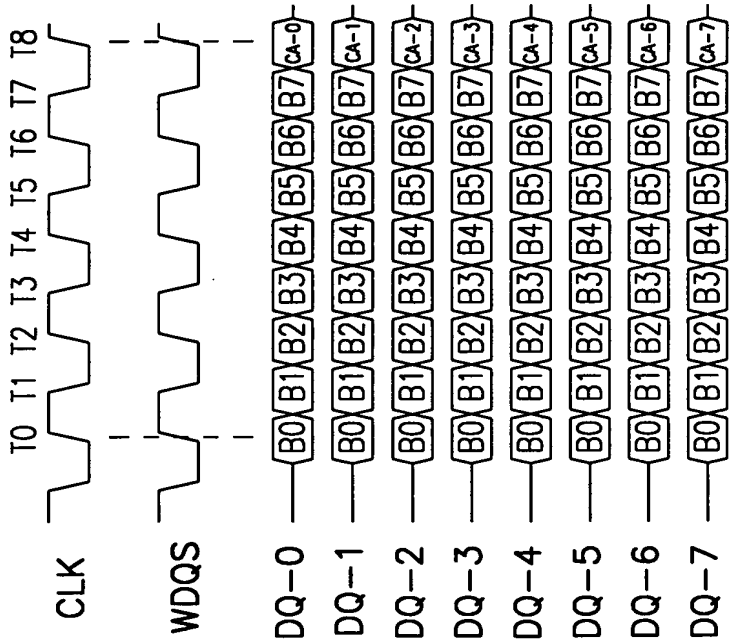

T0 T1 T2 T3 T4 T5 T6 T7 T8
CLK
WDQS
DQ-0
DQ-1
DQ-2
DQ-3
DQ-4
DQ-5
DQ-6
DQ-7
B0 B1 B2 B3 B4 B5 B6 B7
CA-0
CA-1
CA-2
CA-3
CA-4
CA-5
CA-6
CA-7

FIG. 20

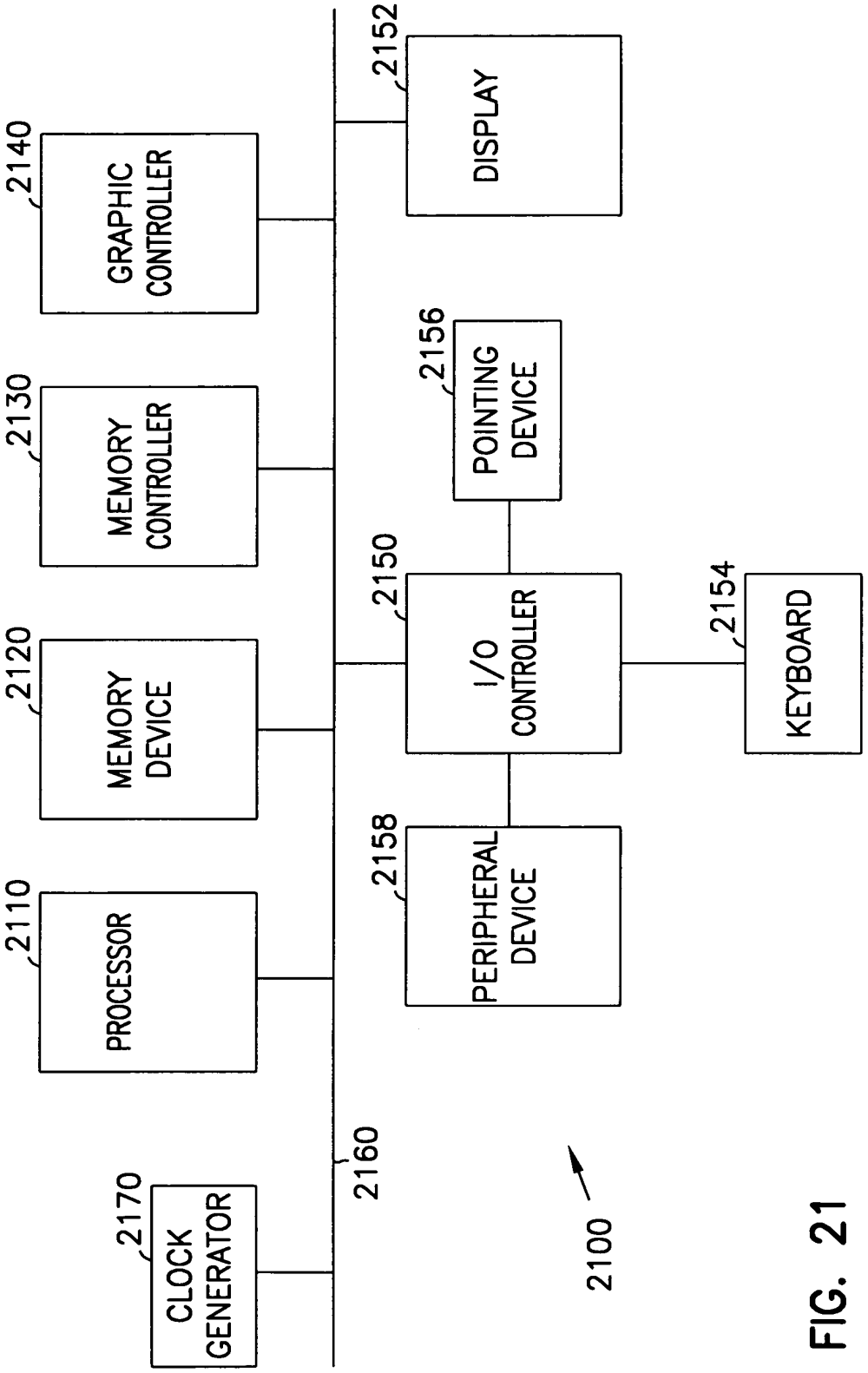

2140
GRAPHIC CONTROLLER
2130
MEMORY CONTROLLER
2120
MEMORY DEVICE
2110
PROCESSOR
2170
CLOCK GENERATOR
2160
2152
DISPLAY
2156
POINTING DEVICE
2150
I/O CONTROLLER
2154
KEYBOARD
2158
PERIPHERAL DEVICE
2100

FIG. 21